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TRANSMITTAL FORM

(to be used for all correspondence after initial filing)

Application No.	09/262,458
Filing Date	March 4, 1999
First Named Inventor	Brian D. Possley
Group Art Unit	2814
Examiner Name	N. Ngo
Attorney Docket Number	42390P6643

Total Number of Pages in This Submission: 23

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ENCLOSURES *(check all that apply)*

- [x] Fee Transmittal Form
  - [ ] Fee Attached
- [ ] Amendment / Response
  - [ ] After Final
  - [ ] Affidavits/declaration(s)
- [x] Extension of Time Request
- [ ] Express Abandonment Request
- [ ] Information Disclosure Statement
- [ ] Certified Copy of Priority Document(s)
- [ ] Response to Missing Parts/ Incomplete Application
  - [ ] Response to Missing Parts under 37 CFR 1.52 or 1.53
- [ ] Assignment Papers *(for an Application)*
- [ ] Drawing(s)
- [ ] Licensing-related Papers
- [ ] Petition
- [ ] Petition to Convert a Provisional Application
- [ ] Power of Attorney, Revocation Change of Correspondence Address
- [ ] Terminal Disclaimer
- [ ] Request for Refund
- [ ] CD, Number of CD(s)
- [ ] After Allowance Communication to Group
- [ ] Appeal Communication to Board of Appeals and Interferences
- [x] Appeal Communication to Group *(Appeal Notice, Brief, Reply Brief)*
- [ ] Proprietary Information
- [ ] Status Letter
- [ ] Other Enclosure(s) *(please identify below)*:

Remarks

SIGNATURE OF APPLICANT, ATTORNEY, OR AGENT

Firm or Individual name	Gregory D. Caldwell, Reg. No. 39,926 BLAKELY, SOKOLOFF, TAYLOR & ZAFMAN LLP
Signature	[signature]
Date	February 8, 2002

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FEE TRANSMITTAL for FY 2002

Patent fees are subject to annual revision.

☐ Applicant claims small entity status. See 37 CFR 1.27.

TOTAL AMOUNT OF PAYMENT ($) 1,960.00

Complete if Known	
Application Number	09/262,458
Filing Date	March 4, 1999
First Named Inventor	Brian D. Possley
Examiner Name	N. Ngo
Group/Art Unit	2814
Attorney Docket No.	42390p6643

METHOD OF PAYMENT (check one)

☐ Check ☐ Credit card ☐ Money Order ☐ Other ☐ None
☐ Deposit Account

Deposit Account Number: 02-2666

Deposit Account Name: Blakely, Sokoloff, Taylor & Zafman LLP

The Commissioner is authorized to: *(check all that apply)*

☐ Charge fee(s) indicated below ☐ Credit any overpayments

☐ Charge any additional fee(s) during the pendency of the application

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FEE CALCULATION

1. BASIC FILING FEE

Large Entity Fee Code	Large Entity Fee ($)	Small Entity Fee Code	Small Entity Fee ($)	Fee Description	Fee Paid
101	740	201	370	Utility filing fee	
106	330	206	165	Design filing fee	
107	510	207	255	Plant filing fee	
108	740	208	370	Reissue filing fee	
114	160	214	80	Provisional filing fee	

SUBTOTAL (1) ($)

2. EXTRA CLAIM FEES

		Extra Claims		Fee from below		Fee Paid
Total Claims	-** =		x		=	
Independent Claims	- =		x		=	
Multiple Dependent					=	

Large Entity Fee Code	Large Entity Fee ($)	Small Entity Fee Code	Small Entity Fee ($)	Fee Description
103	18	203	9	Claims in excess of 20
102	84	202	42	Independent claims in excess of 3
104	280	204	140	Multiple Dependent claim, if not paid
109	84	209	42	**Reissue independent claims over original patent
110	18	210	9	**Reissue claims in excess of 20 and over original patent

SUBTOTAL (2) ($)

**or number previously paid, if greater. For Reissues, see below

FEE CALCULATION (continued)

3. ADDITIONAL FEES

Large Entity Fee Code	Large Entity Fee ($)	Small Entity Fee Code	Small Entity Fee ($)	Fee Description	Fee Paid
105	130	205	65	Surcharge - late filing fee or oath	
127	50	227	25	Surcharge - late provisional filing fee or cover sheet.	
139	130	139	130	Non-English specification	
147	2,520	147	2,520	For filing a request for *ex parte* reexamination	
112	920*	112	920*	Requesting publication of SIR prior to Examiner action	
113	1,840*	113	1,840*	Requesting publication of SIR after Examiner action	
115	110	215	55	Extension for reply within first month	
116	400	216	200	Extension for reply within second month	
117	920	217	460	Extension for reply within third month	
118	1,440	218	720	Extension for reply within fourth month	
128	1,960	228	980	Extension for reply within fifth month	1,960.00
119	320	219	160	Notice of Appeal	
120	320	220	160	Filing a brief in support of an appeal	
121	280	221	140	Request for oral hearing	
138	1,510	138	1,510	Petition to institute a public use proceeding	
140	110	240	55	Petition to revive - unavoidable	
141	1,280	241	640	Petition to revive - unintentional	
142	1,280	242	640	Utility issue fee (or reissue)	
143	460	243	230	Design issue fee	
144	620	244	310	Plant issue fee	
122	130	122	130	Petitions to the Commissioner	
123	50	123	50	Prosessing fee under 37 CFR 1.17(q)	
126	180	126	180	Submission of Information Disclosure Stmt	
581	40	581	40	Recording each patent assignment per property (times number of properties)	
146	740	246	370	Filing a submission after final rejection (37 CFR § 1.129(a))	
149	740	249	370	For each additional invention to be examined (37 CFR § 1.129(b))	
179	740	279	370	Request for Continued Examination (RCE)	
169	900	169	900	Request for expedited examination of a design application	

Other fee (specify) ______

* Reduced by Basic Filing Fee Paid

SUBTOTAL (3) ($) 1,960.00

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SUBMITTED BY

Complete (if applicable)

Name *(Print/Type)*	Gregory D. Caldwell	Registration No. *(Attorney/Agent)*	39,926	Telephone	(503) 684-6200
Signature				Date	02/08/02

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IN THE UNITED STATES PATENT AND TRADEMARK OFFICE
BEFORE THE BOARD OF PATENT APPEALS AND INTERFERENCES

26/Appeal Brief
Theresa
3-20-02

In re Patent Application of:

Possley

Application No.: 09/262,458

Filed: March 4th, 1999

For: GATE ARRAY ARCHITECTURE

OIPE JC156
FEB 26 2002
PATENT & TRADEMARK OFFICE

Examiner: N. Ngo

Art Unit: 2814

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Washington, D.C. 20231

APPEAL BRIEF
IN SUPPORT OF APPELLANT'S APPEAL
TO THE BOARD OF PATENT APPEALS AND INTERFERENCES

Dear Sir:

Applicant (hereinafter "Appellant") hereby submits this Brief in triplicate in support of his Appeal from a final decision by the Examiner in the above-captioned case. Appellant respectfully requests consideration of this Appeal by the Board of Patent Appeals and Interferences for allowance of the claims in the above-captioned patent application.

An oral hearing is not requested.

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The PTO did not receive the following listed item(s) Check $300

TABLE OF CONTENTS

I. REAL PARTY IN INTEREST

The invention is assigned to Intel Corporation of 2200 Mission College Boulevard, Santa Clara, California 95052.

II. RELATED APPEALS AND INTERFERENCES

To the best of Appellant's knowledge, there are no Appeals or Interferences related to the present appeal, which will directly affect, be directly affected by, or have a bearing on the Board's decision.

III. STATUS OF THE CLAIMS

Claims 1-11, 21-26, and 44 are under final rejection and remain pending in the above-referenced patent application. Claims 13-20 have been withdrawn from consideration and will be pursued in a separate continuation application. Claims 27-43 have been allowed and have been refiled in a separate continuation application to permit them to proceed to issuance without delay. The Examiner confirmed his final rejection in an Advisory Action mailed on June 1, 2001.

The claims stand rejected under 35 U.S.C 103(a) as being unpatentable over Tran at al. (hereinafter "Tran"; US Patent No. 5,780,883); in view of Sato (US Patent 4,816,887).

IV. STATUS OF THE AMENDMENTS

There are no outstanding amendments pending for the above-referenced patent application.

V. SUMMARY

As is well-known, gate array architectures are commonly used for many types of integrated circuit designs. In this context, the term gate array architecture refers to a repeated pattern of transistors embedded in a semiconductor or silicon substrate. Employing a gate array architecture stands in contrast to the custom design of the layout of transistors on a silicon or semiconductor substrate, which is also accomplished using CAD/CAM techniques. Use of gate array architectures offers the advantage of quicker or shorter fabrication and throughput time, lower costs and ease in making fixes or logic changes after a chip design has already been completed.

In a gate array architecture design approach, the layout of the silicon or semiconductor is determined before metallization routing is determined. Gate array architectures are employed in the silicon or semiconductor that are standard arrays of transistors that may be designed using the appropriate metallization to form many different types of circuits. Therefore, while the silicon is being fabricated in a manufacturing facility to produce the gate arrays of transistors in the silicon, the design of the remaining portion of the chip, such as the portion interconnecting the transistors, continues to occur. While resulting in a less customized chip, this approach has the advantage of shorter turn around time in terms of chip production because, while portions of the chip are being manufactured, the remaining portion of the chip is still being designed. Thus, the overall time to design and manufacture the chip is reduced. For the gate array approach, the chip design, as with the customized or, as it is sometimes referred to, the standard cell approach, once the gate array cells are appropriately designed, again, an APR tool is employed to interconnect the metallization of the different cells.

Traditional gate array architectures employ what is commonly referred to as a "sea of transistors" or a "sea of gates" architecture. This means that the gate array base comprises a regularly repeating pattern of individual or group transistors. Having a large number of generic transistors is desirable so that any one of a large number of possible logic functions may be implemented by customizing the metallization above the array. A drawback of this approach is that by offering only a simple, generic transistor pattern, resulting logic implementation is suboptimal in terms of certain technical issues, such as density, power and/or performance.

More recent examples of gate array architectures attempt to address this problem by using a complex base structure comprising many different sizes and configurations of transistors. While this may achieve improved results in terms of density, for example, it may also restrict both synthesis and layout flexibility because the CAD/CAM tools are restricted to using exactly this predetermined mix of different base sites. Furthermore, as shall be explained in more detail hereinafter, such configurations result in undesirable amounts of power consumption compared with embodiments in accordance with the present invention.

Layout of the metallization and vias is typically performed using computer-aided design and computer-aided manufacturing tools. Typically, these tools execute on a system, such as a computer or similar computing platform, in which the circuit designer or other technical personnel design logic cells. Once the logic cells are designed, CAD/CAM tools are then further employed to automatically place and route interconnections between these cells in order to produce the layout for the overall integrated circuit chip. As previously indicated, the systems or tools employed to perform this operation are often referred to as automatic placement and routing or APR systems or tools. A tape is usually produced that contains a data set and/or other electronically stored information which is used by equipment employed to process the silicon, and directs the operations of the equipment to produce the chip.

FIG. 3 is a diagram illustrating an embodiment of a flip-flop implemented using functional block elements, such as multiplexors and inverters. For example, flip-flop 300 includes multiplexors 310 and 340 and inverters 320, 330, 350, 360, 370, 410 and 420. As illustrated, this implementation includes a data input port 315, a clock signal input port 415 and an output signal port 355. Of course, output signal port 355 provides "Q bar" (QB), which is an inverted output signal produced by the flip-flop. Alternatively or in addition, the output signal Q could be provided.

In this embodiment the clock signal that is applied to the input port is applied to internal clock buffer circuits that are implemented as inverters 410 and 420. An issue that arises when implementing a flip-flop using a gate array, such as a traditional gate array architecture, is the overall power consumption that results from charging a capacitive load, such as a load associated with internal clock buffers 410 and 420. For example, as shall be explained in more detail hereinafter, if these internal clock buffers were implemented using smaller transistors, this would result in a lower power consumption, as is generally desirable. Of course, the difficulty is accomplishing this using a "sea of transistors" traditional gate array architecture.

An embodiment of a gate array architecture, such as the embodiment illustrated in FIG. 2, complements a traditional "sea of transistors" gate array with small transistors, such as on the order of one-third the size of full-sized transistors, in this particular embodiment, for example. This allows the

creation of integrated circuit chips with a lower overall power consumption without the additional design overhead associated with customized circuitry, as previously described. The functional hardware configuration to implement the internal clock buffering for sequential cells, such as clock buffering circuits 410 and 420, is illustrated in FIG. 3 and in greater detail in FIG. 4

The energy employed to charge a capacitive load is given by equation 1 below.

$$E = CV^2 \qquad [1]$$

where E is energy, C is capacitance, and V is voltage.

From this equation, it is apparent that a reduction in the individual capacitive load reduces the energy consumed by the same factor, thus resulting in a lower overall consumption. From examining FIG. 4, it may be inferred that the power saving per cell is realized from the lower input capacitance on CLK, CLK' and CLK", resulting in a lower switching power per cell.

FIG. 2 is a plan diagram illustrating an embodiment of a layout of a gate array architecture in accordance with the present invention. This particular gate array architecture includes a capacitance improved layout. Therefore, each row of "regular" or full" sized transistors, the larger transistors is this embodiment, is complemented with row of "small" transistors, the smaller transistors in this embodiment, which may be used for clock buffering and to create logic gates that will consume less power compared with full or regular sized transistors. Therefore, in this particular embodiment, two separate and distinct sizes of transistors are employed so that the smaller of the two may be applied to operations that typically consume significant or greater amounts of power.

An integrated circuit including a metallization layer formed for a gate array architecture embodiment in accordance with the present invention includes the benefits previously described of a traditional gate array architecture approach, however, without the larger power consumption typically associated with the traditional gate array architecture approach. As previously described, the nature of a traditional gate array architecture is to provide a sea of generic transistors which are then interconnected with metallization to implement a given logic function. This approach allows quick development times that, however, typically result in greater power consumption due to the presence of

full size transistors for clock buffering, for example. This higher power consumption of a traditional gate array design may become a significant contributor to the cost of a part as densities of integrated circuits increase and it becomes more difficult, therefore, and more costly to dissipate heat in such an environment. The capacitive load reduced gate array architecture of this embodiment, previously described, also uses an array of regular or full sized transistors; however, to achieve better power consumption, the regular sized transistors are complemented with rows of "small" devices which may then be configured as the internal clock buffer for the cell, as previously described. Therefore, this particular embodiment has the benefits of a traditional gate array architecture with the additional benefit of low power consumption.

The table illustrated in FIG. 5 compares the simulated power consumption resulting in switching the clock signal applied to the input port of a flip-flop using a variety of gate array architecture techniques. Techniques that are compared include the embodiment illustrated in FIG. 2, the embodiment illustrated in FIG. 1, and a technique used in a commercially available product produced by Silicon Architects (SiArc), of Palo Alto, CA, known as Cell-Based Array (CBA). As illustrated, the embodiment illustrated in FIG. 2 produces the lowest power consumption among these approaches, although, it is expected that a customized cell may be designed to reduce power consumption further. Another reason the approach in this particular embodiment is particularly desirable is that flip-flops typically are a significant proportion of the functional blocks employed in typical integrated circuit (IC) chips. For example, typically, approximately 20 percent or more of total cells of a digital IC may be flip-flops, which may use 50 percent or more of the total cell area of the IC.

The embodiment of a gate array architecture illustrated in FIG. 2 includes a semiconductor substrate having a plurality of N-type diffusion regions and P-type diffusion regions. Furthermore, as illustrated in FIG. 2, these diffusion regions have partially overlaying polysilicon landing types to form N-type and P-type transistors. The regions are relatively-sized to form two distinct transistor sizes in this particular embodiment, smaller N-type and P-type transistors and larger N-type and P-type transistors. In the embodiment illustrated in FIG. 1, the successive rows of small diffusion regions, two in this embodiment, are followed by successive rows of regular or full-sized diffusion regions, two in this

embodiment. The immediately successive rows in the two differently sized-regions in this particular embodiment have opposite polarity. Furthermore, as illustrated, the polysilicon landing sites from these smaller and larger regions are not connected or coupled. Figure 5 illustrates a layout for metallization to implement the circuit shown in FIG. 3 using the embodiment shown in FIG. 1, although, of course, the invention is not limited in scope to this particular layout or to the embodiment illustrated in FIG. 1. As illustrated, ovals denote connections between layers, squares denote vias, thick black lines denote the metal one layer interconnect, and the thin black lines denote the metal two layer interconnect.

Although the invention is not limited in scope in this respect, the relative capacitance of the larger and smaller relatively sized transistors for the embodiment illustrated in FIG. 2 is on the order of one-third, that is, the small transistors have approximately one-third the capacitance of the full or regular-sized transistors, corresponding to the relative transistor size. As previously indicated, once the gate array architecture is formed in silicon, an interconnect is formed overlying the gate array architecture. For an integrated circuit implementing the circuit illustrated in FIG. 3, the interconnect formed is adapted to connect the transistors of the gate array architecture to form a flip-flop. Furthermore, for the embodiment illustrated in FIG. 1, the interconnect is further adapted to connect the transistors of the gate array architecture so that the internal clock buffers of the flip-flop, such as those illustrated in FIG. 4 for this particular embodiment, for example, are formed from the smaller transistors.

As previously suggested, this particular embodiment may be repeated throughout an integrated circuit chip and employed to implement a variety of functional elements for the overall chip. Such an integrated circuit chip employing this particular embodiment of a gate array architecture, may typically be included on a motherboard that is incorporated in a personal computer, such as a lap top or desk top computer, although the invention is not limited in scope in this respect. Likewise, it might be employed in a communication device, such as a pager or cell phone, or, alternatively, in a computer peripheral, just to provide a few additional examples. For example, FIG. 7 is a schematic diagram illustrating an embodiment 710 of an IC in accordance with the present invention. As illustrated, embodiment 710 is incorporated in unit 700, that may comprise a computer, a computer peripheral, a communication device, or another platform that may employ such an embodiment.

The invention, of course, is not limited in scope to a particular technique for fabricating an integrated circuit chip that includes an embodiment of a gate array architecture in accordance with the present invention. However, typically, a silicon or semiconductor substrate is processed to form a gate array architecture of transistors in the substrate prior to the formation of the metallization interconnect. As previously described, this is one of the advantages of employing a gate array architecture. A variety of techniques for processing a silicon or semiconductor substrate to form the gate array architecture may be employed. Furthermore, typically the polysilicon landing sites are formed as part of the gate array architecture, for the embodiment illustrated in FIG. 1, for example. Once the gate array architecture has been fabricated, a metallization interconnect may be formed overlying the gate array architecture. Additional background information about semiconductor manufacturing technology is provided, for example, in "CMOS Processing Technology," Chapter 3 of the aforementioned <u>Principles of CMOS VLSI Design</u> by N. Weste and K. Eshraghian.

Another advantage of this particular embodiment of a gate array architecture in accordance with the present invention, as previously described, is that it may be stored as a data file, for example. Where the gate array architecture is employed in this fashion, an article, such as a storage medium comprising, for example, a disk or hard drive, may have instructions stored thereon. The instructions, when executed, such as by a computer or similar computing platform, result in the capability being available to design the layout of an integrated circuit chip for fabrication. In this particular embodiment, of course, the integrated circuit chip includes a gate array architecture having relatively sized regions to form two distinct sizes of transistors, smaller N- and P-type transistors and larger N- and P-type transistors. The additional features previously described may also be designed with this capability.

VI. ISSUES PRESENTED

A. Whether the combination of Tran and Sato fails to meet all the limitations of the rejected claims.

B. Whether Tran and Sato are improperly combined.

VII. GROUPING OF CLAIMS

For the purposes of this appeal:

Claims 1-11, 21-26, and 44 stand or fall as Group I.

VIII. ARGUMENT

A. THE COMBINATION OF TRAN AND SATO DOES NOT PROVIDE DIFFUSION REGIONS HAVING PARTIALLY OVERLYING POLYSILICON LANDINGS WHERE AT LEAST ONE OF THE REGIONS FORMS BOTH N-TYPE AND P-TYPE TRANSISTORS.

The Examiner has rejected claims 1-11, 21-26, and 44 under 35 U.S.C. 103(a) (GROUP I) as being unpatentable under Tran in view of Sato. This rejection by the Examiner was traversed during prosecution.

Appellant begins with Claim 1. It recites:

"An integrated circuit comprising:

a gate array architecture;

said gate array architecture including a semiconductor substrate having a plurality of N-type diffusion regions and P-type diffusion regions;

said diffusion regions having partially overlying polysilicon landing sites, at least one forming N-type and P-type transistors;

wherein the regions are relatively-sized to form two distinct transstor sizes, smaller N- and P-type transistors and larger N- and P-type transistors."

It is respectfully asserted that with respect to the claims, claim 1, for example, the Examiner has failed to meet the elements required to show a _prima facie_ case of obviousness, as outlined in the US Patent and Trademark Office's own Manuel of Patent Office Examiner and Procedure (MPEP), section 2143. As indicated by that section, it is well-established that to establish a _prima facie_ case of obviousness, the Examiner must first show a suggestion or motivation to modify the prior art or to combine two or more prior art documents. Additionally, there must be a reasonable expectation of success in combining or modifying the prior art documents(s). Finally, the prior art documents(s) must teach or suggest all of the claim limitations.

However, even if one were to assume that it was appropriate to combine the patents cited by the Examiner, which Appellant disputes in the next section of this appeal brief, nonetheless, the combination of Tran and Sato still fails to teach or suggest all the claim limitations of, for example, claim 1. It is, therefore, respectfully asserted that the Examiner has failed to make a *prima facie* case of obviousness with respect to claim 1. Therefore, claim 1 is in a condition for allowance, and Appellant respectfully requests that the Board overrule and remand this case to the Examiner with instructions to enter an allowance regarding claim 1, and as explained below, the remaining rejected claims.

Appellant has already argued in prosecution that claim 1 distinguishes from the cited patents by reciting **diffusion regions having partially overlying polysilicon landing sites, at least one forming N-type and P-type transistors**. The Examiner, however, has attempted to rely on FIG. 8 of Tran in his rejection. Nonetheless, an inspection of that figure reveals quite clearly that **any given diffusion region in FIG. 8 of Tran forms either N-type transistors or P-type transistors, but not both types transistors for a single diffusion region**. In particular, Tran states, at column 6, lines 14-17, about FIG. 8: "The base row type 140 includes two voltage rails 142 and 144 and four diffusion strips **that alternate between P- and N-channel diffusion strips.**" (emphasis added)

In addition to being a patentably distinguishable difference between the patents cited by the Examiner and the language of claim 1 above, as Appellant has previously argued in prosecution. The approach of Tran is, furthermore, disadvantageous. Specifically, the approach introduces significant additional design complexity.

The significance of this additional complexity cannot be understated. **As one example of such additional complexity, Tran would require additional layers of metallization to connect N-type and P-type transistors.** There are many potential disadvantages that would follow from additional layer(s)of metalization including, additional manufacturing cost to provide the extra layer(s) of metalization, additional reliability issues from the presence of more layer(s) of metal that may rust or corrode, additional power consumption due to current flowing through additional layer(s) of metallization during circuit operation, and additional non-ideal capacitive and inductive effects due to such current flow in the additional metal layer(s) that may, during circuit operation, degrade overall circuit

performance. Again, this is intended to highlight only some of the potential disadvantages associated with the approach in Tran, rather than provide an exhaustive list.

In the face of this rather compelling set of issues that would indicate the rejection by the Examiner was misplaced, the Examiner, in the Final Office Action, dated March 7, 2001, has attempted to take a position that relies on the combination of Tran and Sato, rather than FIG. 8 alone. In this regard, the Examiner states in that action: "Sato discloses in figure 9 that one gate can be formed on both N-type and P-type transistors. Therefore, it would have been obvious to one of ordinary skill in the art to form the polysilicon gate of Tran on both N-type and P-type transistors as taught by Sato." However, it is respectfully asserted that this asserted combination is insufficient.

As indicated above, contrary to the Examiner's position, the combination would fail to produce the claimed subject matter as recited in claim 1. More specifically, and as explained more fully below, the combination still fails to provide ***diffusion regions having partially overlying polysilicon landing where at least one of the regions forms both N-type and P-type transistors.***

By this argument, the Examiner is attempting to use Sato to provide the aspect of claim 1 that Tran is clearly missing; however, neither Tran nor Sato, either individually or in combination, provides a polysilicon landing site overlying diffusion regions to form both N-type and P-type transistors. **In particular, the Examiner has pointed to FIG. 9 of Sato, as indicated above. However, FIG. 9 of Sato is not relevant at all. To the contrary, FIG. 9 is a circuit diagram of a Random Access M mory (RAM) cell. To be clear, whereas the figure pointed to in Tran provides a gate architecture layout diagram of the type that might be useful to one of ordinary skill in the art in this context, FIG. 9, by contrast, is simply a circuit diagram. As a simple inspection of FIG. 9 will reveal, in contrast to, for example, FIG. 5 of the above-referenced patent application (or FIG. 8 of Tran, as mentioned just previously), such a circuit diagram provides no information regarding gate architecture layout that might be relevant to address the limitation of claim 1 not shown in Tran. A circuit diagram does not and cannot illustrate the layout to fabricate a cell using p lysilic n landings and diffusion regions.** Therefore, even if one of ordinary skill in the art were to combine Tran and Sato, it would fail to produce the claimed subject matter, as recited in claim

1. **<u>At best, th combinati n of Tran and Sat , even assuming the c mbination is pr p r, which is disputed below, sh ws polysilic n landings ov rlying ither N-type diffusi n r gions r P-type diffusion r gions, not overlying at least one diffusion regi n wher both both N-type and P-type transistors are formed.</u>**

As previously indicated, one advantage of the approach recited in claim 1 is that design complexity is reduced. For example, additional layers of metallization to connect the N-type and P-type transistors are avoided. However, one of ordinary skill in the art would not be able to produce this result simply from the asserted combination of Sato and Tran. Claim 1, therefore, patentably distinguishes from the cited patents and is allowable.

Claims 2-11 and 44 depend from and include all limitations of claim 1. Therefore, these claims patentably distinguish from the cited patents for at least the same reasons. It is therefore respectfully requested that the Board also overrule and remand the rejection of these claims to the Examiner with instructions to allow these claims.

Claim 21 includes a similar limitation as the limitation disputed in claim 1. Therefore, this claim patentably distinguishes from the cited patents for at least the same reasons. Likewise, claims 22-26 depend from and include all the limitations of claim 21 and patentably distinguish from the cited patents.

Therefore, all of these claims, claims 1-11, 21-26, and 44, patentably distinguish from the cited patents. It is therefore respectfully requested that the Board overrule the Examiner and remand this case with instructions to the Examiner to enter an allowance of the rejected claims.

B. **THE EXAMINER HAS ALSO PROVIDED NO EVIDENCE OF MOTIVATION OR SUGGESTION IN THE ART FOR THE PROPOSED COMBINATION.**

As discussed above, it is respectfully asserted that with respect to the claims, claim 1, for example, the Examiner has failed to meet the elements required to show a *prima facie* case of obviousness, as outlined in the US Patent and Trademark Office's own Manuel of Patent Office Examiner and Procedure (MPEP), section 2143. As indicated by that section, it is well-established that to establish a *prima facie* case of obviousness, the Examiner must first show a suggestion or motivation to modify the prior art or to combine two or more documents. Additionally, there must be a reasonable expectation of success in combining or modifying the prior art documents(s). Finally, the prior art documents(s) must teach or suggest all the claim limitations. However, Tran and Sato is not a proper combination because one of ordinary skill in the art would not be motivated to make it. As is well-established Federal Circuit law, there must be a motivation shown in the prior art for the combination. Here, such a motivation has not been demonstrated.

Specifically, the Examiner has failed to show a suggestion or motivation to modify the teachings of Tran or to combine the teachings of Tran with Sato (or any other prior art documents) in order to make a device as claimed by Appellant. As stated in *In re Kotzab, 217 F.3d 1365, 1370 (Fed. Cir 2000),* "[t]here must be a showing of suggestion or motivation to modify the teachings of that reference."

Tran is directed to **a gate array architecture for a *multiplexer circuit*.** Sato, on the other hand, is directed to **a gate array architecture for a *RAM cell*.** Therefore, one of ordinary skill in the art would not attempt to combine these to produce the invention as recited, for example, in claim 1. **Furthermore, there is no teaching, or even suggestion, in either Tran or Sato, that, by employing a polysilicon landing over both P-type and N-type diffusion regions in a gate array architectur , additional layers of metallization may be avoided. Therefore, the required motivation for the combinati n has not been provided.** As stated in *In Re Rouffet, 47 USPQ2d 1453, 1457-58 (Fed. Cir. 1998)*, "[T]he examiner must show reasons that the skilled artisan, confronted with the same

problems as the inventor and with no knowledge of the claimed invention, would select the elements from the cited prior art references for combination in the manner claimed."

It appears that Tran and Sato are not only directed to address different problems. They are also directed to different problems than addressed by above-referenced patent application. As indicated above, Tran is specifically directed to a gate array architecture for a multiplexer circuit. Likewise, Sato is specifically directed to a gate array architecture for a RAM cell. Although the gate array architecture in the above-referenced patent application might be employed to produce such functional circuits, that is not its focus or purpose. Claim 1, therefore, patentably distinguishes from the cited patents and is allowable.

Claims 2-11 and 44 depend from and include all limitations of claim 1. Therefore, these claims patentably distinguish from the cited patents for at least the same reasons. It is therefore respectfully requested that the Board also overrule and remand the rejection of these claims to the Examiner with instructions to allow these claims.

Claim 21 includes a similar limitation as the limitation disputed in claim 1. Therefore, this claim patentably distinguishes from the cited patents for at least the same reasons. Likewise, claims 22-26 depend from and include all the limitations of claim 21 and patentably distinguish from the cited patents.

Therefore, all of these claims, claims 1-11, 21-26, and 44, patentably distinguish from the cited patents. It is therefore respectfully requested that the Board remand the rejection of all of these claims to the Examiner with instructions to allow them.

IX. CONCLUSION

In view of the foregoing, it is respectfully asserted that all claims pending in this application are in condition for allowance. Appellant respectfully request that the Board of Patent Appeals and Interferences overrule the Examiner, and direct allowance of all pending claims in this application.

This brief is submitted in triplicate, along with a check for $300.00 to cover the appeal fee for one other than a small entity as specified in 37 C.F.R. § 1.17(c).

Respectfully Submitted By

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X. APPENDIX A: CLAIMS ON APPEAL

1. An integrated circuit comprising: a gate array architecture;

said gate array architecture including a semiconductor substrate having a plurality of N-type diffusion regions and P-type diffusion regions; said diffusion regions having partially overlying polysilicon landing sites, at least one forming N-type and P-type transistors;

wherein the regions are relatively-sized to form two distinct transistor sizes, smaller N- and P-type transistors and larger N- and P-type transistors.

2. The integrated circuit of claim 1, wherein the ratio between the two distinct transistor sizes is on the order of one-third.

3. The integrated circuit of claim 2, wherein the ratio between the capacitance of the larger and smaller relatively sized transistors is on the order of one-third.

4. The integrated circuit of claim 1, wherein said partially overlying polysilicon landings for the smaller and larger transistors are not connected.

5. The integrated circuit of claim 4, and further comprising an interconnect overlying said gate array architecture;

the interconnect being adapted to connect the transistors of the gate array architecture to form a flip-flop.

6. The integrated circuit of claim 5, wherein the interconnect is further adapted to connect the transistors of the gate array architecture so that the internal clock buffers of the flip-flop are formed from the smaller transistors.

7. The integrated circuit of claim 6, wherein said gate array architecture is repeated in said integrated circuit.

8. The integrated circuit of claim 6, wherein said integrated circuit is incorporated in a communications device.

9. The integrated circuit of claim 6, wherein said integrated circuit is attached to a motherboard.

10. The integrated circuit of claim 9, wherein said integrated circuit is in incorporated in a personal computer.

11. The integrated circuit of claim 10, wherein said personal computer comprises one of a laptop and a desktop computer.

21. An article comprising: a storage medium, said storage medium having instructions stored thereon, said instructions, when executed, resulting in the capability to design the layout of an integrated circuit chip for fabrication, the integrated circuit chip including a gate array architecture, the gate array architecture comprising a plurality of N-type diffusion regions and P-type diffusion regions;

said diffusion regions having partially overlying polysilicon landing sites, at least one forming N-type and P-type transistors;

wherein the regions are relatively-sized to form two distinct transistor sizes, smaller N- and P-type transistors and larger N- and P-type transistors.

22. The article of claim 21, wherein said instructions, when executed, result in the capability to design the layout of the gate array architecture, wherein the ratio between the two distinct transistor sizes is on the order of one-third.

23. The article of claim 22, wherein said instructions, when executed, result in the capability to design the layout of the gate array architecture, wherein said partially overlying polysilicon landings for the smaller and larger transistors are not connected.

24. The article of claim 23, wherein said instructions, when executed, result in the capability to design the layout of a metallization interconnect overlying said gate array architecture.

25. The article of claim 24, wherein said instructions, when executed, result in the capability to design the layout of a metallization interconnect overlying said gate array architecture, wherein said metallization interconnect couples the transistors of the gate array architecture to form a flip-flop.

26. The article of claim 25, wherein said instructions, when executed, result in the capability to design the layout of a metallization interconnect overlying said gate array architecture that connects the transistors of the gate array architecture so that the internal clock buffers of the flip-flop are formed from the smaller transistors.

44. The integrated circuit of claim 1, wherein successive rows of small diffusion regions are followed by successive rows of regular-sized diffusion regions;

wherein immediately successive rows within similarly-sized diffusion regions have opposite polarity.